Fig. 1

Prior art

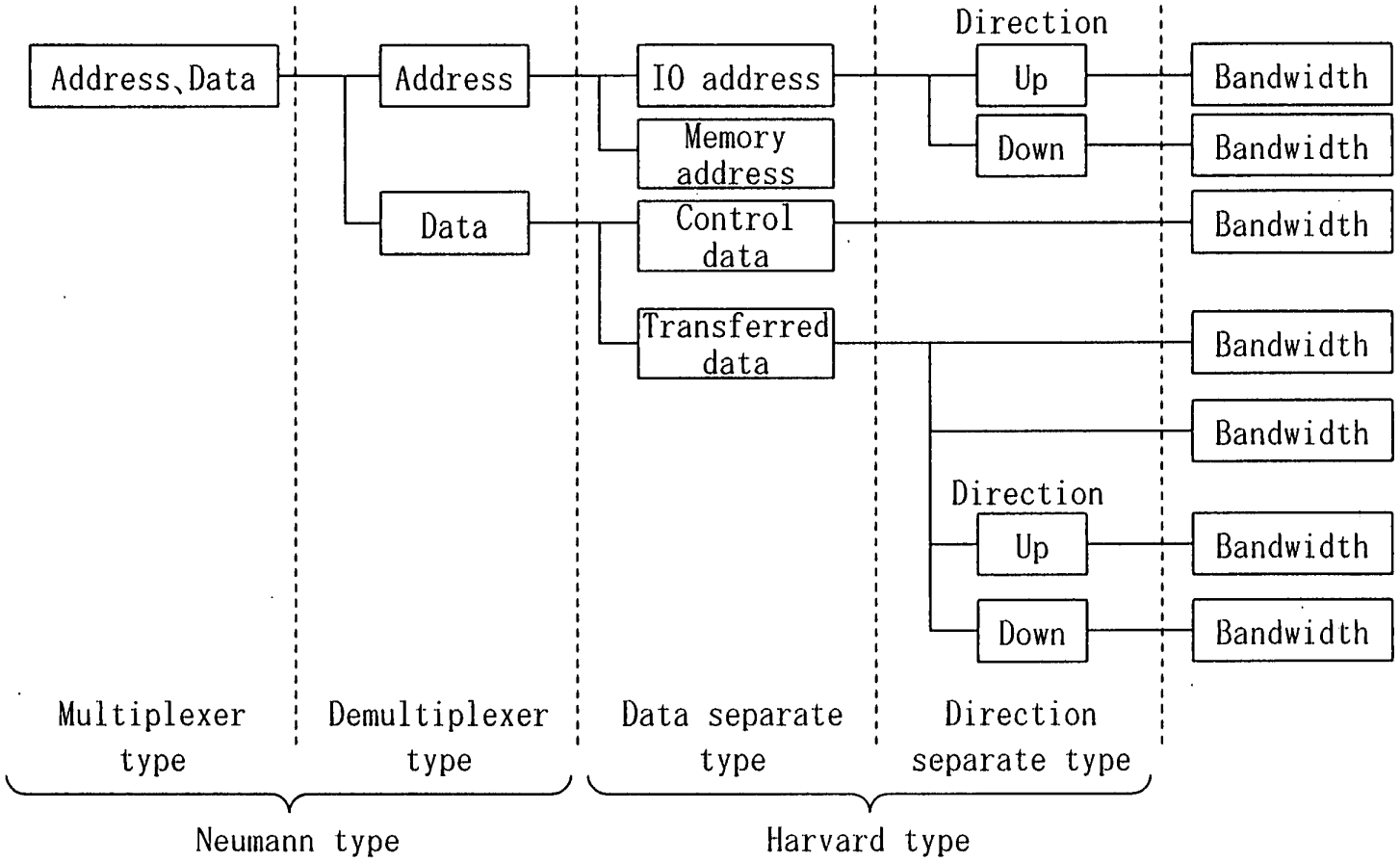


Fig. 2(a)

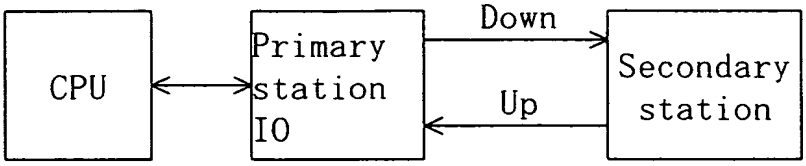


Fig. 2(b)

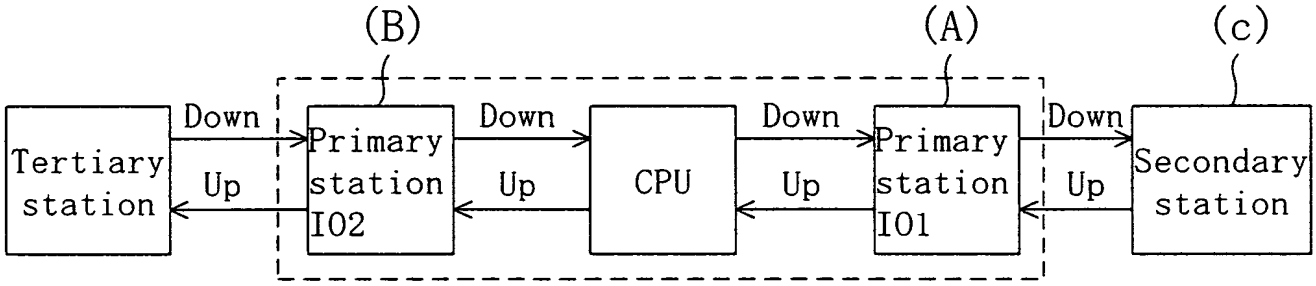


Fig. 2(c)

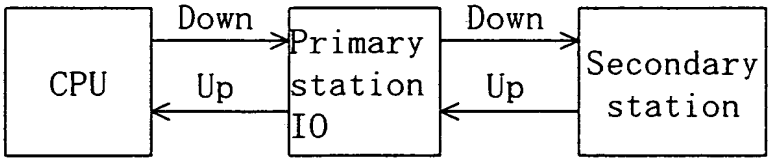


Fig. 3(a)

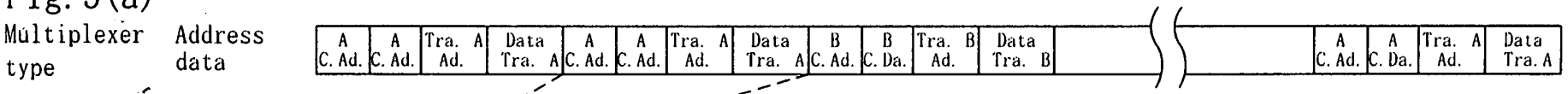


Fig. 3 (b)

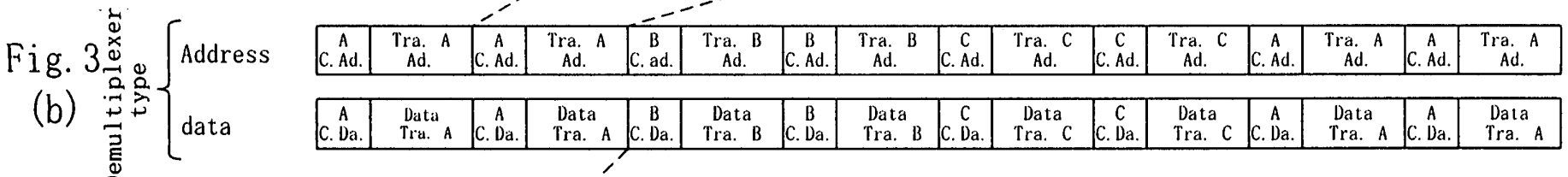


Fig. 3 (c)

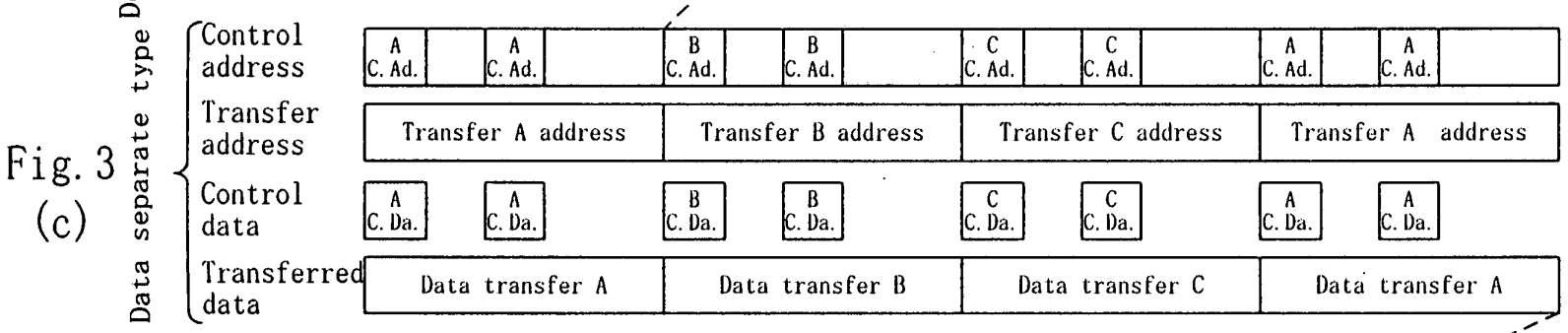


Fig. 3 (d)

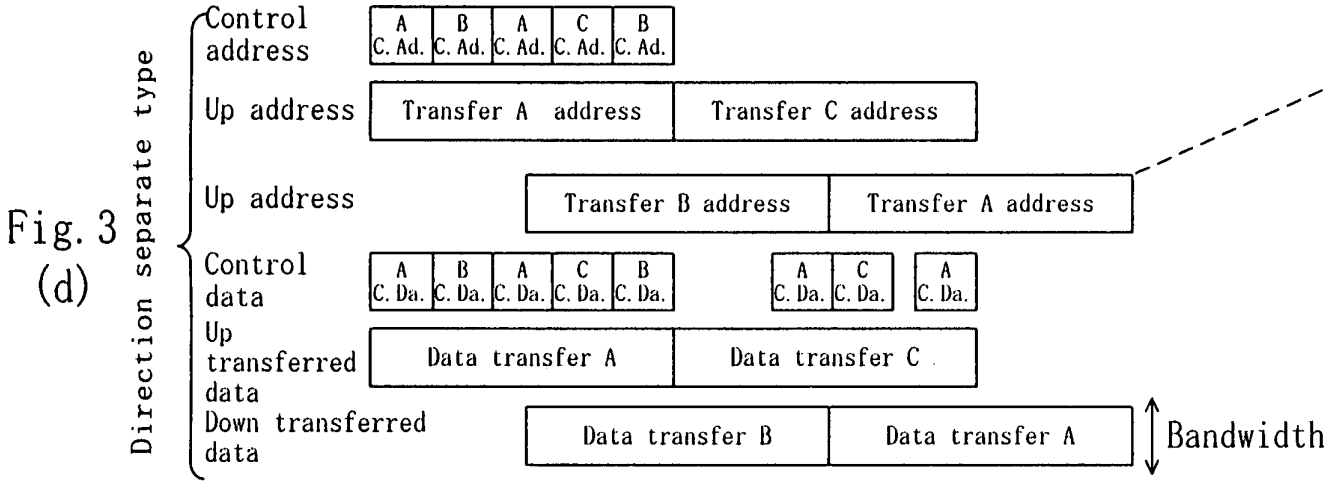


Fig. 4

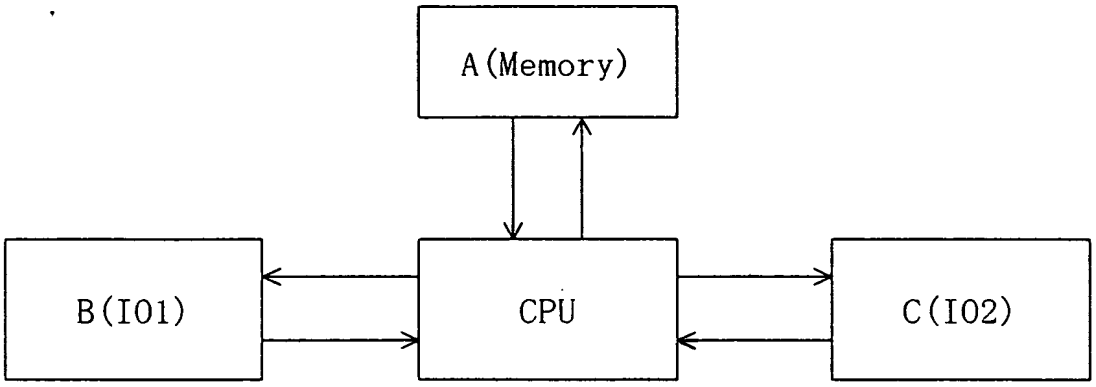


Fig. 5(a)

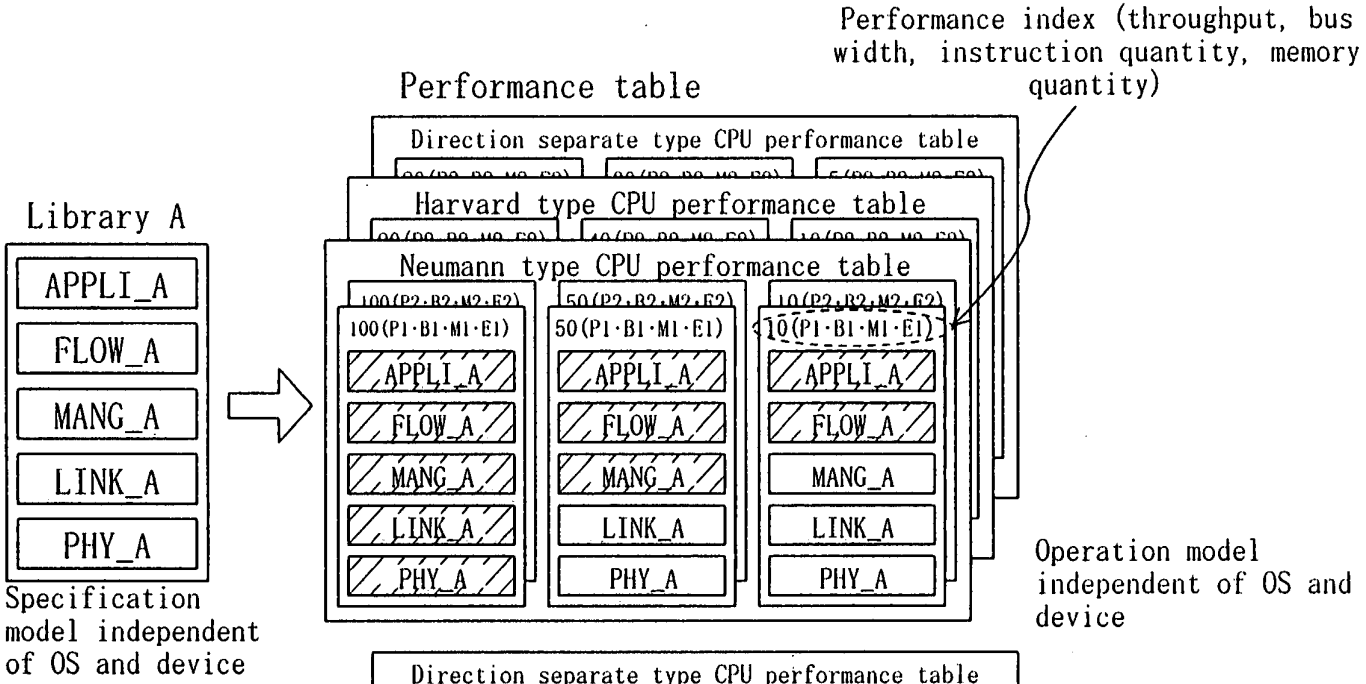

Performance index (throughput, bus width, instruction quantity, memory quantity)
Performance table
Direction separate type CPU performance table
Harvard type CPU performance table
Neumann type CPU performance table
100(P1·B1·M1·E1)
50(P1·B1·M1·E1)
10(P1·B1·M1·E1)
APPLI_A
FLOW_A
MANG_A
LINK_A
PHY_A
Library A
APPLI_A
FLOW_A
MANG_A
LINK_A
PHY_A
Specification model independent of OS and device
Operation model independent of OS and device

Fig. 5(b)

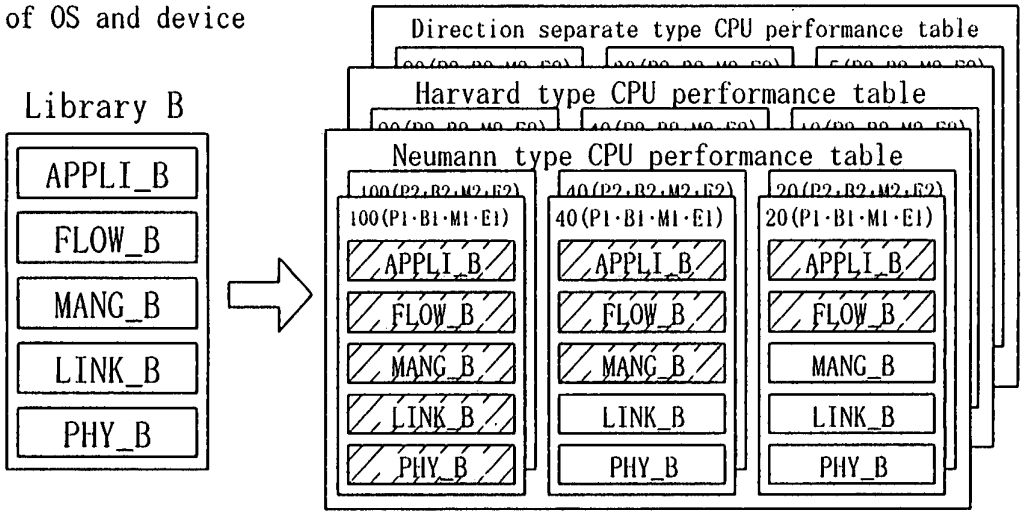

Direction separate type CPU performance table
Harvard type CPU performance table
Neumann type CPU performance table
100(P1·B1·M1·E1)
40(P1·B1·M1·E1)
20(P1·B1·M1·E1)
APPLI_B
FLOW_B
MANG_B
LINK_B
PHY_B
Library B
APPLI_B
FLOW_B
MANG_B
LINK_B
PHY_B

Fig. 6

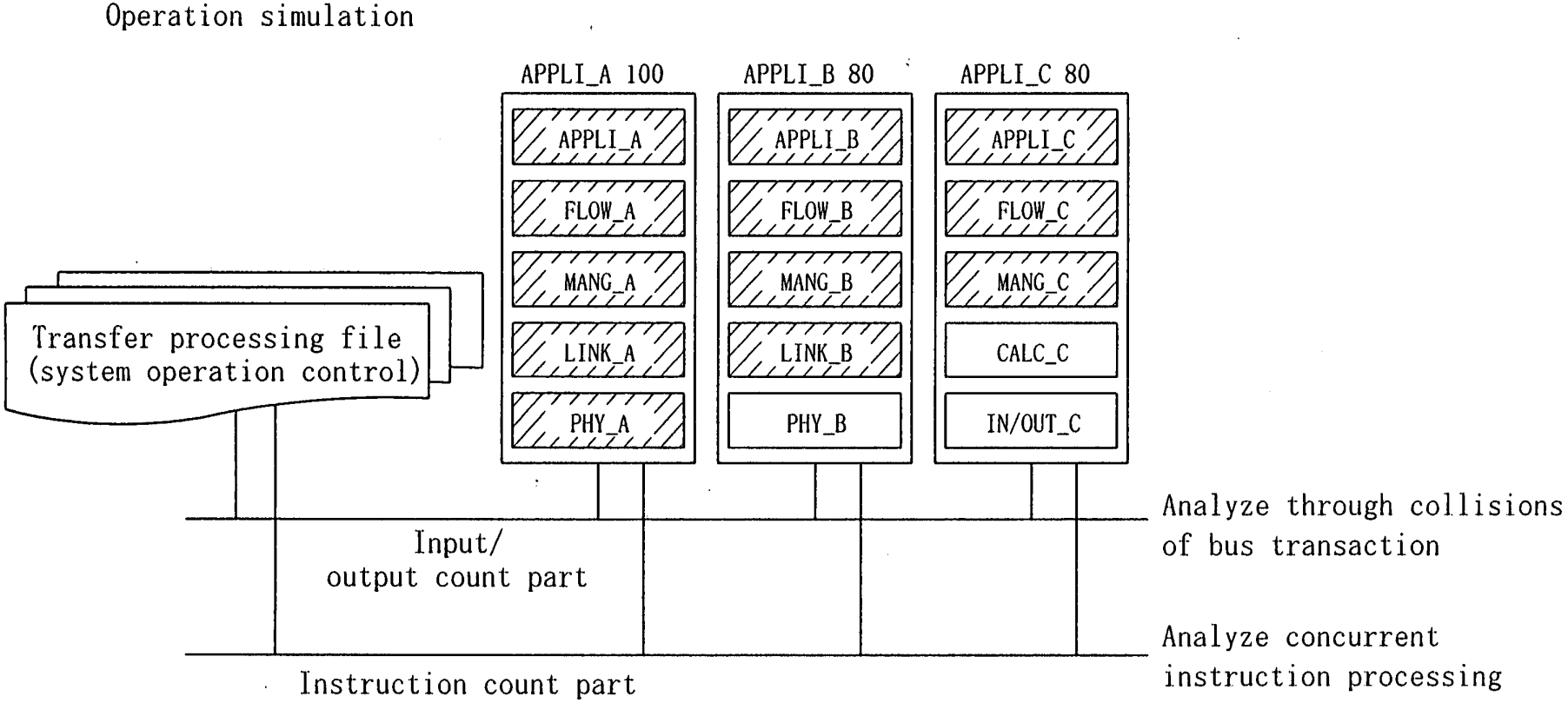

Operation simulation
APPLI_A 100
APPLI_B 80
APPLI_C 80
APPLI_A
FLOW_A
MANG_A
LINK_A
PHY_A
APPLI_B
FLOW_B
MANG_B
LINK_B
PHY_B
APPLI_C
FLOW_C
MANG_C
CALC_C
IN/OUT_C
Transfer processing file
(system operation control)
Input/
output count part
Instruction count part
Analyze through collisions
of bus transaction
Analyze concurrent
instruction processing

Fig. 7

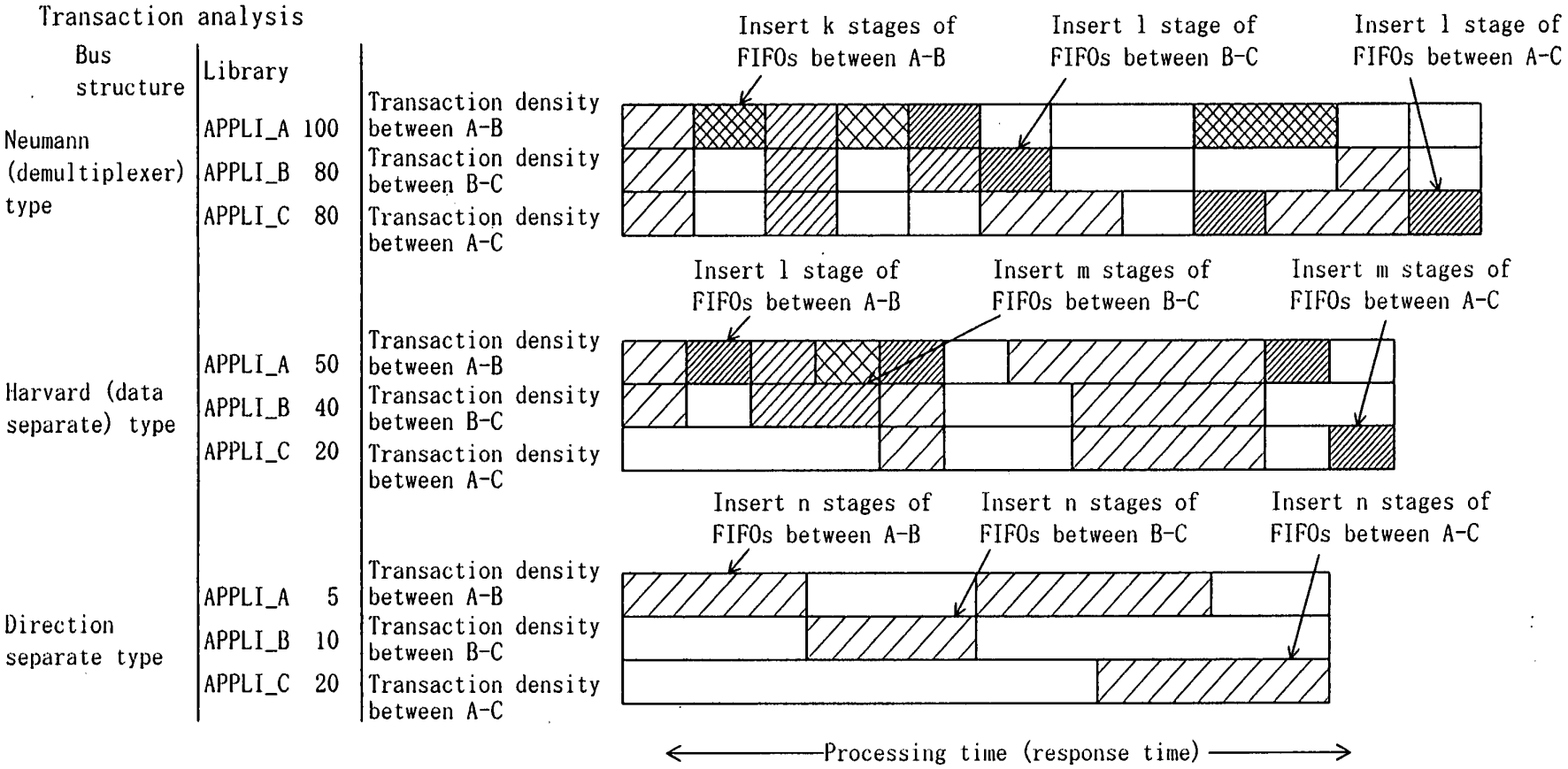

Transaction analysis
Bus structure
Library
Neumann (demultiplexer) type
APPLI_A 100
APPLI_B 80
APPLI_C 80
Transaction density between A-B
Transaction density between B-C
Transaction density between A-C
Insert k stages of FIFOs between A-B
Insert l stage of FIFOs between B-C
Insert l stage of FIFOs between A-C
Harvard (data separate) type
APPLI_A 50
APPLI_B 40
APPLI_C 20
Transaction density between A-B
Transaction density between B-C
Transaction density between A-C
Insert l stage of FIFOs between A-B
Insert m stages of FIFOs between B-C
Insert m stages of FIFOs between A-C
Direction separate type
APPLI_A 5
APPLI_B 10
APPLI_C 20
Transaction density between A-B
Transaction density between B-C
Transaction density between A-C
Insert n stages of FIFOs between A-B
Insert n stages of FIFOs between B-C
Insert n stages of FIFOs between A-C
Processing time (response time)

Fig. 8

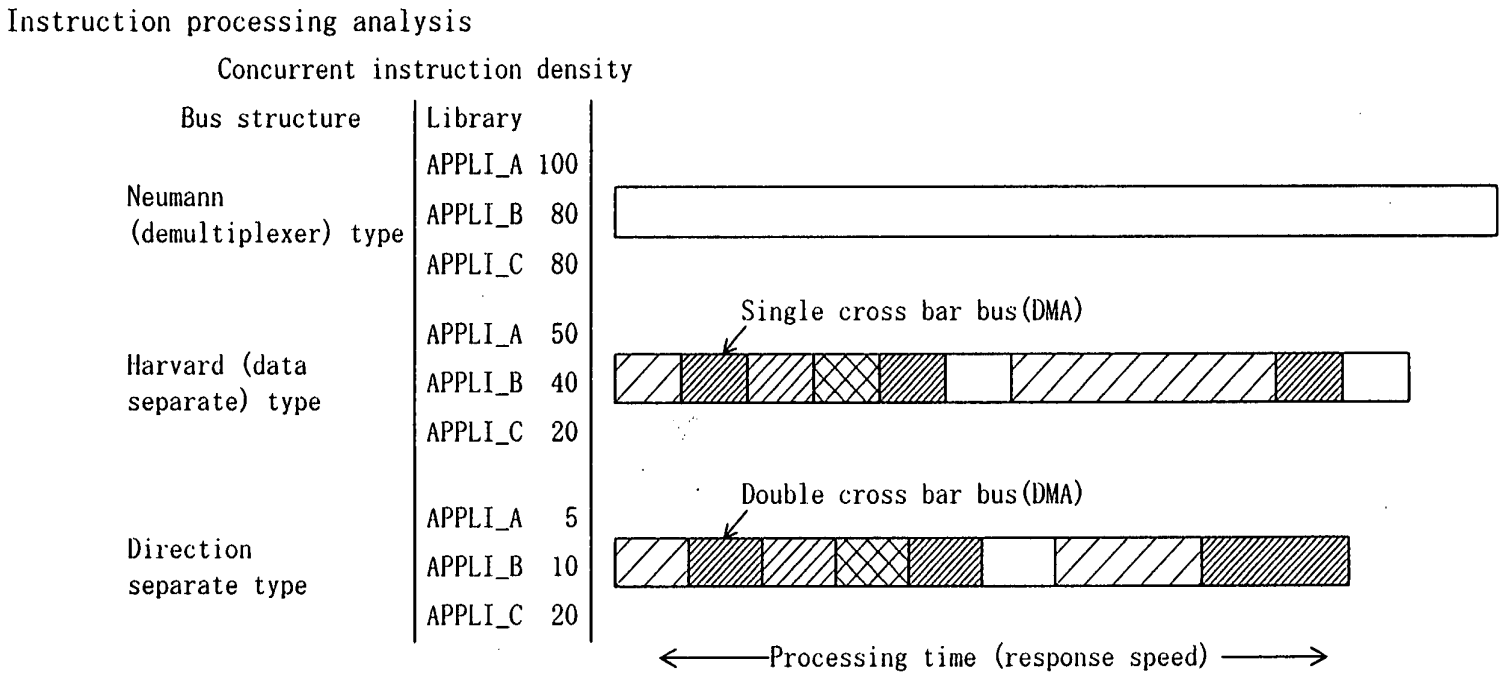

Instruction processing analysis
Concurrent instruction density
Bus structure
Library
Neumann (demultiplexer) type
APPLI_A 100
APPLI_B 80
APPLI_C 80
Harvard (data separate) type
APPLI_A 50
APPLI_B 40
APPLI_C 20
Direction separate type
APPLI_A 5
APPLI_B 10
APPLI_C 20
Single cross bar bus(DMA)
Double cross bar bus(DMA)
Processing time (response speed)

Fig. 9

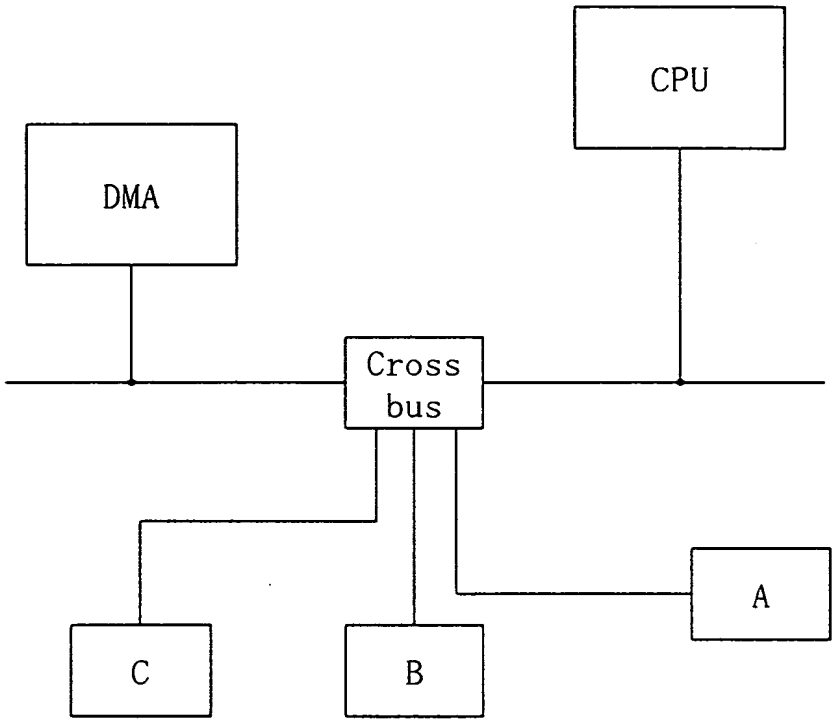


Fig. 10(a)

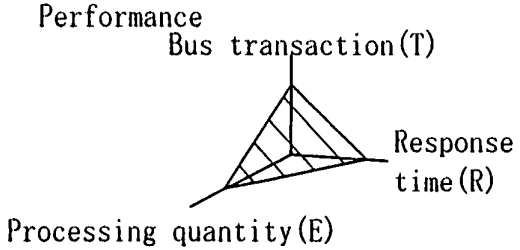


Fig. 10(b)

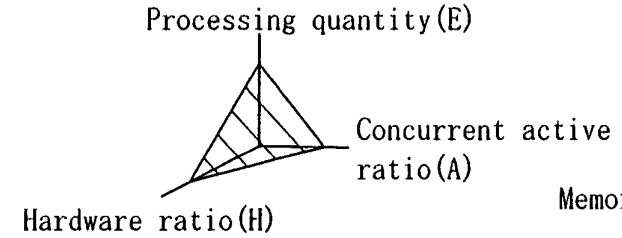
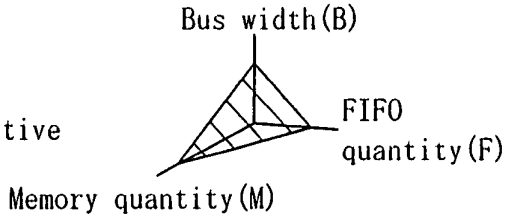


Fig. 10(c)



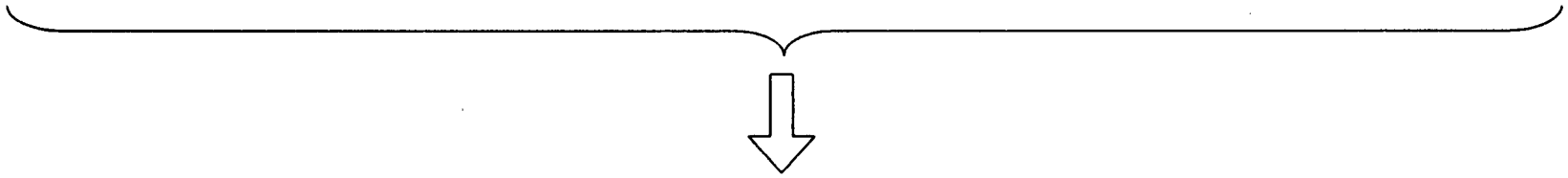
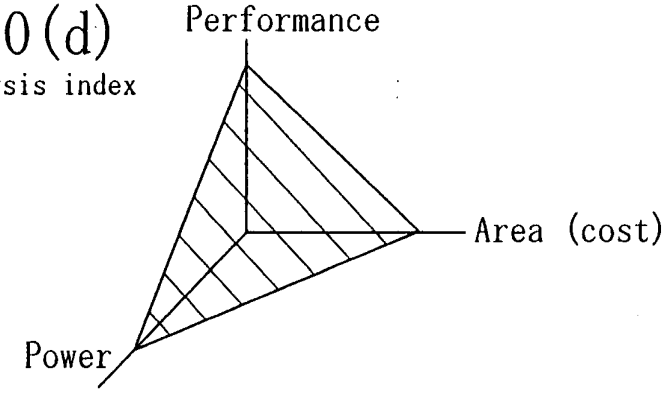


Fig. 10(d)



Analysis index (weighted index)

Fig. 11 (a) Basis for determining performance index

Response time: R
Performance affecting coefficient of response time: lx
Bus transaction: T
Performance affecting coefficient of bus transaction: mx
Processing quantity: E
Performance affecting coefficient of processing quantity: nx
Rlx × Tmx × En = Performance index: x
Example) lx = 1/1 sec., mx = 1/10 times, nx = 1/10 MIPS

Fig. 11 (b) Basis for determining power index

Average (maximum) processing quantity: Eav (Emx)
Power affecting coefficient of processing quantity: ly
Hardware ratio: H
Power affecting coefficient of hardware ratio: my
Average (maximum) concurrent active ratio: Anv (Amx)
Power affecting coefficient of concurrent active ratio: ny
or Eav ly × Hmy × Aavny = Average power index
Emx ly × Hmy × Amxny = Maximum power index } : y
Example) ly = 1/10 MIPS, my = 1/20%, ny = 1/25%

Fig. 11 (c) Basis for determining area index

Memory quantity: M
Area affecting coefficient of memory quantity: lz
FIFO quantity: F
Area affecting coefficient of FIFO quantity: mz
Bus width: B
Area affecting coefficient of bus width: nz
Mlz × Fmz × Bnz = Area index: z
Example) lz = 1/1 kByte, mz = 1/128 bytes, nz = 1/16 bits

Fig. 11 (d)

Basis for determining analysis index

Performance index (performance)
Coefficient affecting performance index: a
Power index (power)
Coefficient affecting power index: b
Area index (area)
Coefficient affecting area index: c
ax + by + cz = Optimal index
Example) a = 0.5 , b = 0.3 , c = 0.2

Fig. 12

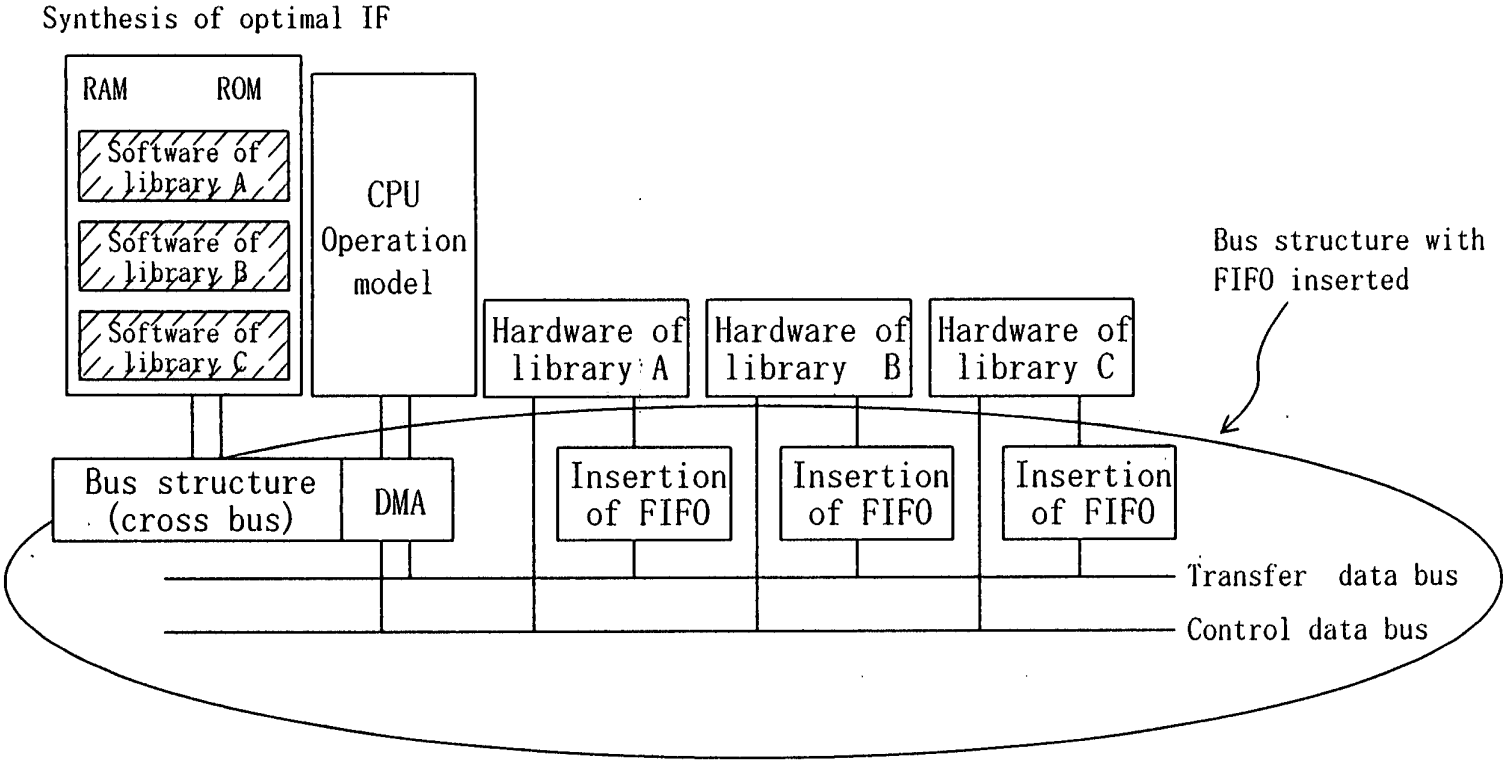
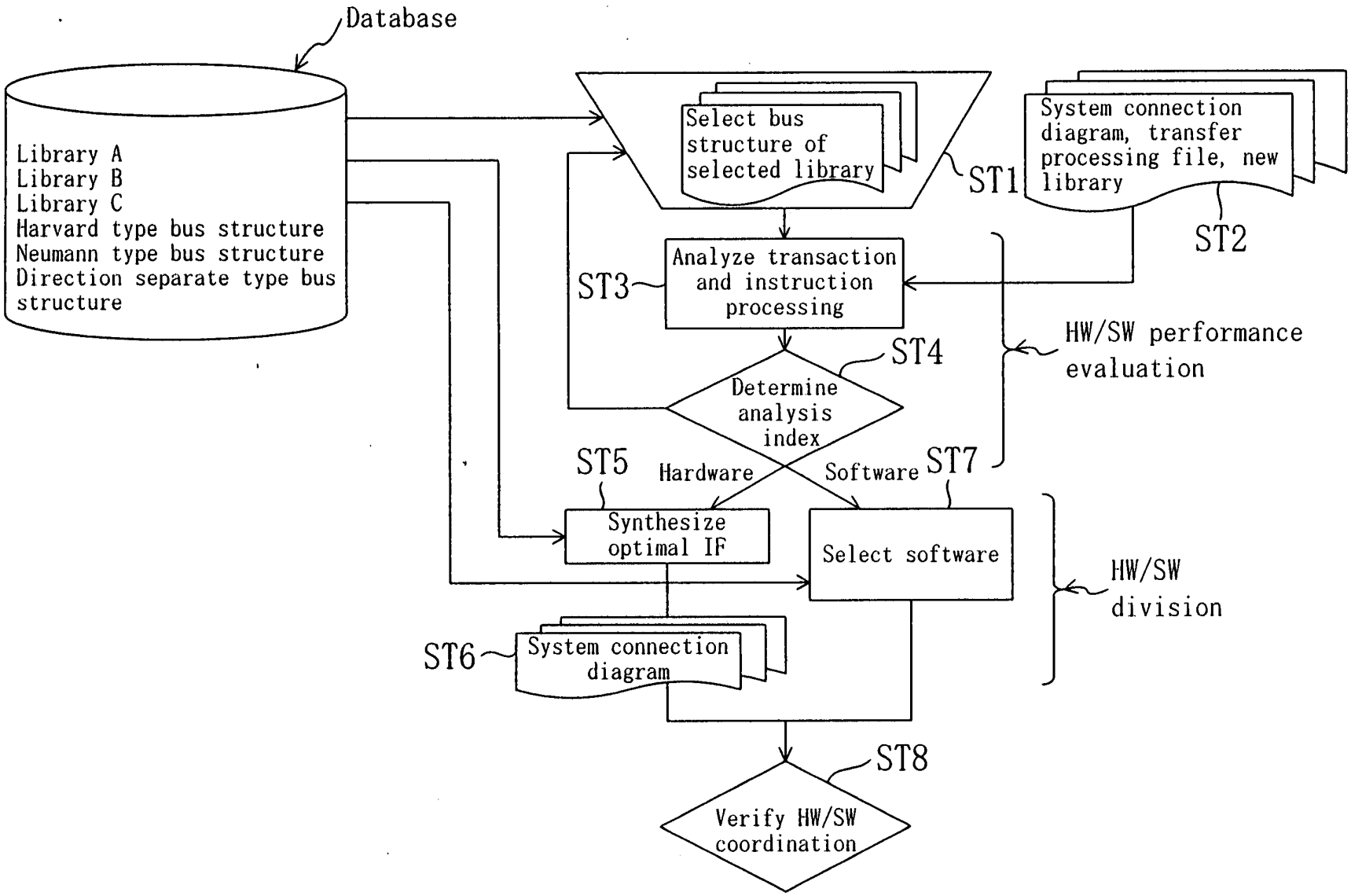

Synthesis of optimal IF
RAM
ROM
Software of library A
Software of library B
Software of library C
CPU Operation model
Hardware of library A
Hardware of library B
Hardware of library C
Bus structure with FIFO inserted
Bus structure (cross bus)
DMA
Insertion of FIFO
Insertion of FIFO
Insertion of FIFO
Transfer data bus
Control data bus

Fig. 13


Database
Library A
Library B
Library C
Harvard type bus structure
Neumann type bus structure
Direction separate type bus structure
Select bus structure of selected library
ST1
System connection diagram, transfer processing file, new library
ST2
Analyze transaction and instruction processing
ST3
ST4
Determine analysis index
HW/SW performance evaluation
ST5
Hardware
Software
ST7
Synthesize optimal IF
Select software
HW/SW division
ST6
System connection diagram
ST8
Verify HW/SW coordination